Amendments to the Specification:

Please replace paragraph [12, 27, 28 and 31-34] with the following amended paragraphs:

[12] However, the background art SDH system processes the asynchronous signal by including the elastic buffer 21, the write pointer generating unit ~~15~~25, the read pointer generating unit 26, and the serial/parallel changing unit 22 in a respective channel. Therefore, as shown in Figure 1, if the background art SDH system processes 84 channels of DS-1 signals, it needs 84 write pointer generating units, read pointer generating units, and serial/parallel changing units, respectively. In addition, in the background art SDH system, the number of gates needed to implement the respective channels are increased in the case of a multiple channel embodiment, whereby the system structure is complex.

[27] Figure 3 is a block diagram showing a serial data mapping apparatus for a synchronous digital hierarchy system according to a preferred embodiment of the present invention. As shown therein, the serial data mapping apparatus comprises an STM-1 address generating unit 41 generating a mapping address stm1 indicating a mapping position of new data; a VC mapping unit 43 for mapping the DS asynchronous signals DS-1, DS-1E, DS3E, and DS4E as VC signals VC11, VC12, VC3, and VC4 according to the mapping address stm1; and an STM-1 formatter 42 for pointer processing and multiplexing a virtual container of the VC signal outputted from the VC mapping unit ~~42~~43, whereby an STM-1 signal is generated.

[28] As shown in Figure 4, the VC mapping unit 43 comprises a plurality of elastic buffers 31 for storing the asynchronous DS-1 signal of 84 channels and DS-1E signals of 63 channels; a write pointer generating unit 32 generating write addresses WA of the elastic buffers 31; a read pointer ~~controlling~~ generating unit 33 generating a read address RA of the elastic buffer 31; a VC1 mapper 34 multiplexing parallel asynchronous data Pd of the byte unit, read in the elastic buffers 31, as VC signals VC11/VC12 according to a format controlling signal; and a VC1 framer 35 for identifying the mapping position of asynchronous signals according to the format address stm1 of the STM-1 address generating unit 41, and controlling operations of the elastic buffers 31, the read pointer ~~controlling~~ generating unit 33, and the VC1 mapper 34 according to the identified mapping position.

[31] The VC1 framer 35 chooses one buffer among the 84 elastic buffers 31 and generates sts1/group/channel SONET addresses for controlling the read pointer ~~controlling~~ generating unit 33. Consequently, a certain elastic buffer 31 is chosen for generating the sts1/group/channel addresses and the read pointer ~~controlling~~ generating unit 33 generates a read address RA and outputs it to the chosen elastic buffer 31.

[32] That is, the read pointer controlling unit 33 does not read the data as a bit unit from the elastic buffer 31, instead it reads the data a byte unit (8 bit). Accordingly, the read pointer ~~controlling~~ generating unit 33 ~~controls a read pointer generating unit (not shown) and~~ outputs a read address, that is, a start bit of 8 bit data to the elastic buffer 31. Then the elastic buffer 31 outputs a parallel asynchronous signal of 8 bits according to the start bit. At that time, the read pointer ~~controlling~~ generating unit 33 increases the read address RA by +8 in order to read the next 8 bits of data.

[33] However, in the asynchronous signals stored in the elastic buffers 31, a STUFF bit, that is, Null data is included as well as the data signal. Therefore the read pointer ~~controlling~~ generating unit ~~35~~ 33 judges whether the read address RA is increased by +8, +6, or by +4 according to controlling signals Ctrlen and ien outputted from the VC1 framer ~~34~~ 35 and, after that, generates a start bit of the read address RA of the asynchronous signal which will be read next time.

[34] Also, the read pointer ~~controlling~~ generating unit 33 controls the operation speed of the read pointer generating unit according to controlling signals Psr and Nsr outputted from the VC1 framer 35. That is, the read pointer ~~controlling~~ generating unit 33 increases by +1 or decreases by –1 the operation speed of the read pointer generating unit according to the

controlling signals Psr and Nsr, which are designating the difference between the read address RA and the write address WA.